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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,748	10/01/2004	Kiran V. Chatty	BUR920040050US1	5747

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EXAMINER	
KITOV, ZEEV	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,748	CHATTY ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 3, 5 - 20* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on July 5, 2005. Claims 9 and 14 are amended. Applicant's Arguments have been given careful consideration but they have been found mostly non-persuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5 - 8, 10 - 13, 15 - 18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 6,556,398) in view of Metz et al. (US 5,400,202). Chen discloses following elements of Claims 7 and 1: an upper and a lower nFET (elements 13 and 15 in Fig.2) connected in series with one another between a pair of power supply rails, a voltage divider (elements C and 20 in Fig.3) configured to bias a gate of the upper nFET to a prescribed value. However, it does not disclose an low frequency filter. Metz et al. disclose the RC circuit (elements C and R in Fig. 4a) connected to a gate of the lower nFET (element 18 in Fig. 4a) and configured to filter out the low frequency signals between at least one power supply rail and the gate of the lower nFET. Metz further discloses delivering the signal communicating the occurrence

of an ESD event to the gate of a second transistor (element 18 in Fig. 6a, while the first transistor is element 50 in Fig. 6a). Both references have the same problem solving area, namely providing ESD protection for the semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Chen solution by adding the low frequency filter according to Metz et al., because as Methz states (col. 6, line 59 – col. 7, line 3), due to a presence of the RC triggering arrangement, the ESD protection circuit is not sensitive to power up event but is sensitive to the ESD events, which is a definite advantage, since upon the power up the ESD circuit will not be activated, and therefore, will not disrupt the power supply to the protected electronics.

Regarding Claim 2, Chen discloses the transistor network including a first nFET and a second nFET (elements 13 and 15 in Fig. 2) connected in series with one another between the voltage source and a ground.

Regarding Claims 5 and 15, Chen discloses the bias network (elements 23 and 26 in Fig. 2), a voltage divider communicating a portion of the voltage from the voltage source to the gate of the first transistor (element 13 in Fig. 2). The voltage performs biasing of the transistor gate.

Regarding Claim 6, Metz et al. disclose the trigger network (elements R and C in Fig. 4a) including the resistor and capacitor configured to filter out non-electrostatic discharge events. The RC trigger circuit reacts and activates the clamp only for the transients rising faster than the RC element time constant, while the resistive voltage divider of Chen can be triggered by slow rising and even steady voltage; therefore

presence of the RC trigger circuit makes the clamp reacting only to the transients. A motivation for modification of the primary reference is the same as above.

Regarding Claim 8, Chen discloses the gate of the upper nFET being biased to a prescribed fraction of a voltage between the pair of power supply rails (depending on ratio of the elements 23 and 25 in Fig. 2 resistances).

Regarding Claim 10, Chen discloses the voltage divider having at least one resistor (col. 3, lines 42 - 50).

Regarding Claim 11, Metz et al. disclose the low frequency filter (elements C and R in Fig. 4a) communicating with the source and drain of the lower nFET. The RC element is directly connected to the drain of the nFET and when it turns on the nFET through its gate, the drain of the nFET is affected as well. This way the RC filter communicates with the drain of the nFET. A motivation for modification of the primary reference is the same as above.

Regarding Claim 12, Chen discloses configuring a gate of the upper transistor (element 13 in Fig. 2) of a transistor network to be biased to a prescribed value (by a voltage divider, elements 23, 25 in Fig. 2). Metz et al. disclose coupling an electrostatic discharge event from the trigger circuit (elements C and 20 in Fig. 3) to a gate of a transistor (element MN in Fig. 3) of the transistor network. In the Chen circuit modified according to Metz et al. the electrostatic discharge event is eventually brought to a gate of the lower transistor, since it is the only uncommitted transistor. A motivation for modification of the primary reference is the same as above.

Regarding Claim 13, Chen discloses biasing the gate of the upper transistor (element 13 in Fig. 2) with a voltage divider (elements 23, 25 in Fig.2) connected between the power rails.

Regarding Claim 16, Chen discloses configuring a gate of the upper transistor of a transistor network connected between power rails to be biased to a prescribed value includes applying a voltage obtained by the voltage divider to the gate of the transistor through one power rail (the Vss rail) of the power rails.

Regarding Claim 17, Chen discloses attaching a bias network between one power rail of the power rails (Vss rail in Fig. 2) and the transistor network (the gate of transistor).

Regarding Claim 18, Metz et al. disclose coupling an electrostatic discharge event to a gate of an lower transistor with a high pass filter (elements C and R in Fig. 4a). A motivation for modification of the primary reference is the same as above.

Regarding Claim 20, Chen discloses configuring at least one power rail of the power rails to be in electrical communication with a voltage source (Vss terminal in Fig. 2), and configuring at least one power rail of the power rails to be in electrical communication with ground (the same terminal Vss in Fig. 2).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Metz et al. and Court Decision *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980). As was stated above, Chen and Metz et al. disclose all the elements of Claims 12 and 18. Regarding Claim 19, Metz discloses the high-pass filter including

elements C and R in Fig. 4a, which with respect to the gate of transistor 18 play a role of the high pass filter by filtering out the low frequencies and passing the high frequencies. Metz further discloses the time constant of the filter as being 1 nanosecond (1 kiloohm resistor with1 picofarad capacitance form a filter with a time constant of 1 nanosecond) rather than 1 microsecond as claim requires. As well known in the art, the condition of passage of the ESD event through the filter requires the front of the ESD event being shorter than the time constant of the filter. On other side, the time constant cannot be too large due to structural and cost limitations. Therefore, the time constant is nothing but the result effective variable. The Court Decision addresses an issue of selecting a value of the result effective variable stating that discovering an optimum value of the result effective variable involves only routine skill in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Chen solution by setting the time constant of the high pass filter to a value of one microsecond, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Metz et al. and Court Decision *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8. As was stated above, Chen and Metz et al. disclose all the elements of Claims1 and 2. However, regarding Claim 3, they do not disclose the third transistor. According to Claim 3, the third transistor is connected in exactly the same way as the first transistor, i.e. just repeating schematically and functionally the first transistor. As to possible effect

of increasing the breakdown voltage due to such inclusion, this feature was already achieved in Chen's circuit by connecting two transistors in series. Therefore, inclusion of the third transistor is nothing but duplication of essential working parts, which according to the Court Decision, involves only routine skill in the art. Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made to add the third transistor connected in the same way as the first transistor, since it has been held that mere duplication of the essential working parts involves only routine skill in the art.

Claims 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Metz et al. and Gelecinskyi et al. (US 4,916,381). As was stated above, Chen and Metz et al. disclose all the elements of Claims 7 and 12. However, regarding Claims 9 and 14, they do not disclose the voltage divider having high impedance. Gelecinskyi et al. disclose the MOSFET (element 62 in Fig. 1B) being biased by a voltage obtained from the voltage divider (elements 71 and 72 in Fig. 1B). The values of the resistors are 15 Kohm and 30 Kohm respectively, which represent the high impedance. Both references have the same problem solving area, namely providing a bias for the gate of the MOSFET. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Chen solution by setting the resistors of the voltage divider at high impedance value, because increase of impedance results in reduction of current consumption and heat dissipation.

Allowable Subject Matter

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

1. According to Applicant allegation, the Metz reference "does not teach or suggest a trigger network configured to communicate the occurrence of an ESD event to the gate of a second transistor" (page 12, lines 8 – 10). However, as Claims 1 and 7 rejection states "Metz further discloses delivering the signal communicating the occurrence of an ESD event to the gate of a second transistor (element 18 in Fig. 6a, while the first transistor is element 50 in Fig. 6a)".

2. Applicant further attacks Chen and Metz reference on the basis that these references individually do not disclose all the elements of the Claims (page 12, lines 11 – 18). In response to Applicant's piecemeal analysis of the references, it has been held that one cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of the references. *In re Keller*, 208 USPQ (CCPA 1981).

3. Applicant further attacks a motivation to combine Chen and Metz references together alleging: "Metz describes an alternative arrangement for the protecting circuit of Chen and fails to provide any teachings or suggestion for modifying Chen" (page 12, line 19 – page 13, line 4). However, Metz provides not an alternative

but complementary solution for the Chen circuit; the Chen circuit reacts to both the ESD and the power-up events, while the Metz solution allows the circuit to be triggered by ESD event only without being triggered by power-up event. This is reflected in the motivation for Claims 1 and 7 rejection stating: "Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Chen solution by adding the low frequency filter according to Metz et al., because as Methz states (col. 6, line 59 – col. 7, line 3), due to a presence of the RC triggering arrangement, the ESD protection circuit is not sensitive to power up event but is sensitive to the ESD events, which is a definite advantage, since upon the power up the ESD circuit will not be activated, and therefore, will not disrupt the power supply to the protected electronics".

4. As to Applicant allegation: "neither Chen not Metz teach or suggest the recited high pass filter, such that the art record fails to provide the requisite motivation or rationale for modifying any proper combination of Chen and Metz that would render claim 19 obvious. Further, Applicants submit that the art of the record fails to provide any teaching or suggestion that, if modified in the manner asserted by the Examiner, Chen would operate in its intended manner" (page 13, lines 4 – 9).

First, Metz does teach the high-pass filter as elements C and R in Fig. 4a, which with respect to the gate of transistor 18 play a role of the high pass filter by filtering out the low frequencies and passing the high frequencies. Therefore, the Examiner did not need the Applicant disclosure for suggestion for including a high pass filter.

Second, the goal of the Chen invention is triggering the transistors to bypass the ESD charge. The Metz invention has the same goal. Being modified according to Metz the Chen invention would not only be able to protect against ESD, but in addition, would be protected against triggering at power-up events.

5. Regarding Claims 3 and 4 rejection, the Applicant alleges that the Examiner mischaracterized Applicant claims. However, in support he recites the limitation of Claim 4: "a voltage divider configured to communicate a portion of the voltage from the voltage source to the gate of the first transistor and the gate of the third nFET", which is not applicable to Claim 3.

6. As to rejection of Claims 9 and 14, the Applicant repeats the same allegation, which has been answered with regard to Claims 1 and 7.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
09/16/2005

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